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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/870,609	05/31/2001	Bret Ronald Olszewski	AUS920000844US1	1789

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EXAMINER	
VO, LILIAN	
ART UNIT	**PAPER NUMBER**
2127	

DATE MAILED: 03/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/870,609	OLSZEWSKI ET AL.	
	Examiner	Art Unit	
	Lilian Vo	2127	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 23 are pending.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 12 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Panwar et al. (US 6,058,466, hereinafter Panwar).

4. Regarding **claims 1, 12 and 23**, Panwar discloses:

a multiprocessor system with many execution resources may be sharing among multiple logical processors on a single integrated circuit chip (col. 5, lines 23 – 26)

determining whether a first logical processor on the first physical processor is idle (col. 8, lines 10 - 13);

determining whether a second logical processor on the first physical processor is busy if the first logical processor is idle (col. 8, lines 11 – 22, col. 15, line 63 – col. 16, line 5); and

relinquishing resources of the first physical processor to the second logical processor if the second logical processor is busy (col. 8, lines 15 – 22, col. 15, line 63 – col. 16, line 5).

With respect to the steps of determining whether a second logical processor on the first physical processor is busy if the first logical processor is idle and relinquishing resources of the first physical processor to the second logical processor if the second logical processor is busy, Panwar discloses that each virtual processor in the active state is assigned exclusive control over some of the shared resources in the functional units of processor 102 (col. 7, lines 54 – 56) and that when a napping virtual processor encounters a cache miss that must be satisfied by main memory …, the virtual processor enters the sleep state (col. 8, lines 11 – 13). During the sleeping state, the virtual processor not only preventing from taking additional resources but it also forced to release resources previously occupied so that other virtual processors may continue execution unimpaired …(col. 8, lines 15 – 22). By removing these instructions, pickers 802a and 802b can move forward to pick instructions from active processes (col. 15, line 63 – col. 16, line 5). In other words, if the system detects any virtual processor is being idle, the virtual processor allocated resources are to be released (deallocated) for use by other active processes in other virtual processor. Hence, it would have been obvious for one of an ordinary skill in the art, to recognize that virtual processors are being monitored to determined if they are in the active (busy) state or in an inactive (idle) state in order for the system to know to release shared resources from the idle virtual processor and allocated them to other busy virtual processors.

5. Claims 2 - 6 and 13 - 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Panwar et al. (US 6,058,466), as applied to claims 1, 12 and 23 above, in view of applicants' admitted prior art (hereinafter AAPA).

6. Regarding **claim 2**, Panwar discloses the step of detecting the first logical processor is idle by determining that the first logical processor is not currently running a job (col. 8, lines 11 – 22, col. 15, line 63 – col. 16, line 5). Panwar however did not clearly disclose the additional limitation as claimed. Nevertheless, the concept of recognizing that the run queue associated with a processor is empty if the processor is not currently running a job, is considered well known and also disclosed in AAPA in specification page 3, lines 11 – 13 (when a logical processor becomes idle and there are no threads waiting in the run queue...). It would have been obvious to one of an ordinary skill in the art, at the time of the invention to incorporate AAPA's teaching to the system of Panwar so that the idle processor can affectively utilize the resources by stealing or acquiring threads from another logical processor's run queue (AAPA: specification 3, lines 15 – 16).

7. Regarding **claims 3 and 4**, as modified Panwar discloses the concept of when a logical processor becomes idle and there is no threads waiting in the run queue, the processor checks for threads to acquire from another processor's run queue (AAPA: specification page 3, lines 11 – 15). It is obvious to one of an ordinary skill in the art, at the time the invention was made, to recognize that if there is any thread waiting in the run queue (not empty), the processor would process it first before consider stealing or acquiring threads from the other processor. As a result, the run queue is not empty if there is thread waiting and by processing the thread, the processor is busy, not idle.

8. Regarding **claims 5 and 6**, as modified Panwar discloses the concept of when a logical processor becomes idle and there is no threads waiting in the run queue, the processor checks for threads to acquire from another processor's run queue and that moving a thread between physical processors is expensive (AAPA: specification page 3, lines 11 – 18). It is obvious to one of an ordinary skill in the art, at the time the invention was made, to recognize that the concept of checking for threads from another processor's run queue also mean a run queue corresponding to a different physical processor as well. As a result, if there is any thread available (waiting) from another run queue, it will be acquired and processed.

9. **Claims 13 – 17** are rejected on the same ground as stated in claims 2 – 6 above.

10. Claims 7, 8 and 18 - 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Panwar et al. (US 6,058,466), as applied to claims 1, 12 and 23 above, in view of AAPA, and further in view of Koning (US Pat. Application Publication 2002/0133530).

11. Regarding **claims 7 and 8**, as modified Panwar discloses that one of the logical processors consumes resources of the physical processor (AAPA: specification page 2, lines 6 – 8: when a thread is dispatched to a logical processor, the thread runs as if it is the only thread running on the physical processor). As modified Panwar did not clearly specify that the other logical processor, which relinquished resource, is having a lower priority. Nevertheless, Koning discloses that when a higher priority task that is ready to run, it preempts a currently running lower priority task (page 7, paragraph 0087). Thus, when the currently running task gives up its

resource to a higher priority task, the current task is lowering its priority. It would have been obvious for one of an ordinary skill in the art, at the time the invention was made, to incorporate this concept to Panwar and AAPA to allow a higher priority task to preempt the lower priority task until its priority is lower (Koning: page 1, paragraph 0004).

12. **Claims 18 – 19** are rejected on the same ground as stated in claims 7 – 8 above.

13. Claims 9 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Panwar et al. (US 6,058,466), as applied to claims 1, 12 and 23 above, in view of AAPA, in view of Koning (US Pat. Application Publication 2002/0133530), and further in view of Welland et al. (US 5,247,677, hereinafter Welland).

14. Regarding **claim 9**, as modified Panwar did not disclose the additional limitation as claimed. Nevertheless, Welland discloses the concept of lowering the priority of the logical processor for a predetermined time period (col. 4, line 62 – col. 5, line 17: task 24c current priority is raised from 12 to 15 making task 24c the highest priority which is to be scheduled for execution and at the end of one time slice, the current priority of task 24c would be decremented). It would have been obvious for one of an ordinary skill in the art, at the time the invention was made, to incorporate this concept to modified Panwar to take an advantage of new priority based scheduling process that does not allow lockout to occur so that all tasks will get to run, even the low priority tasks (Welland: col. 1, lines 41 – 51).

15. **Claim 20** is rejected on the same ground as stated in claim 9 above.

16. Claims 10, 11, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Panwar et al. (US 6,058,466), as applied to claims 1, 12 and 23 above, in view of AAPA, in view of Koning (US Pat. Application Publication 2002/0133530), in view of Welland et al. (US 5,247,677) and further in view of Kimmel et al. (6,105,053, hereinafter Kimmel).

17. Regarding **claim 10**, as modified Panwar did not clearly disclose the additional limitation as claimed. Nevertheless, Kimmel discloses the concept of raising the priority of a processor after a predetermined time period (col. 14, lines 10 – 15). It would have been obvious for one of an ordinary skill in the art, at the time the invention was made, to incorporate Kimmel's teaching to modified Panwar so that a thread group that is queued but not executed for a time period can be serviced accordingly (Kimmel: col. 14, lines 10 – 22).

18. Regarding **claim 11**, as modified Panwar discloses the concept of dispatching a job to the logical processor in response to the raised priority (col. 14, lines 18 – 22, 28 - 36).

19. **Claims 21 and 22** are rejected on the same ground as stated in claims 10 - 11 above.

Response to Arguments

20. Applicant's arguments with respect to claims 1, 2, 10 – 13 and 21 - 22, have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lilian Vo whose telephone number is 571-272-3774. The examiner can normally be reached on Monday - Thursday, 7:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lilian Vo
Examiner
Art Unit 2127

lv
February 18, 2005

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